

What is claimed is:

1. A PLL comprising:
 - a phase detector for periodically comparing an externally inputted clock signal with a frequency of an internal clock signal, and outputting an output signal
 - 5 resulting from phase difference of the two signals;
 - a loop filter for outputting a predetermined voltage in response to an output signal from said phase detector; and
 - a VCO for outputting said internal clock signal having a frequency proportional to said predetermined voltage,
 - 10 wherein said VCO includes a capsule for adjusting the value of capacitance by using an internal control signal.
2. The PLL according to claim 1, wherein said capsule includes a plurality of first capacitors connected in parallel to an output terminal of said VCO.
- 15 3. The PLL according to claim 2, wherein said capsule includes a plurality of first switches connected, between said output terminal and the plurality of said first capacitors, respectively, and to be controlled in response to a plurality of control signals generated by using said internal control signal.
- 20 4. The PLL according to claim 2, wherein said capsule includes a plurality of second capacitors connected in series between output terminals of said VCO.
- 25 5. The PLL according to claim 4, wherein said capsule includes a plurality of second switches configured to be connected between an output terminal and the plurality of said second capacitors, and to be controlled in response to a plurality of control signals generated by using said internal control signal.
- 30 6. The PLL according to claim 5, wherein the plurality of said second switches is connected in parallel between an output terminal and the plurality of said second capacitors.